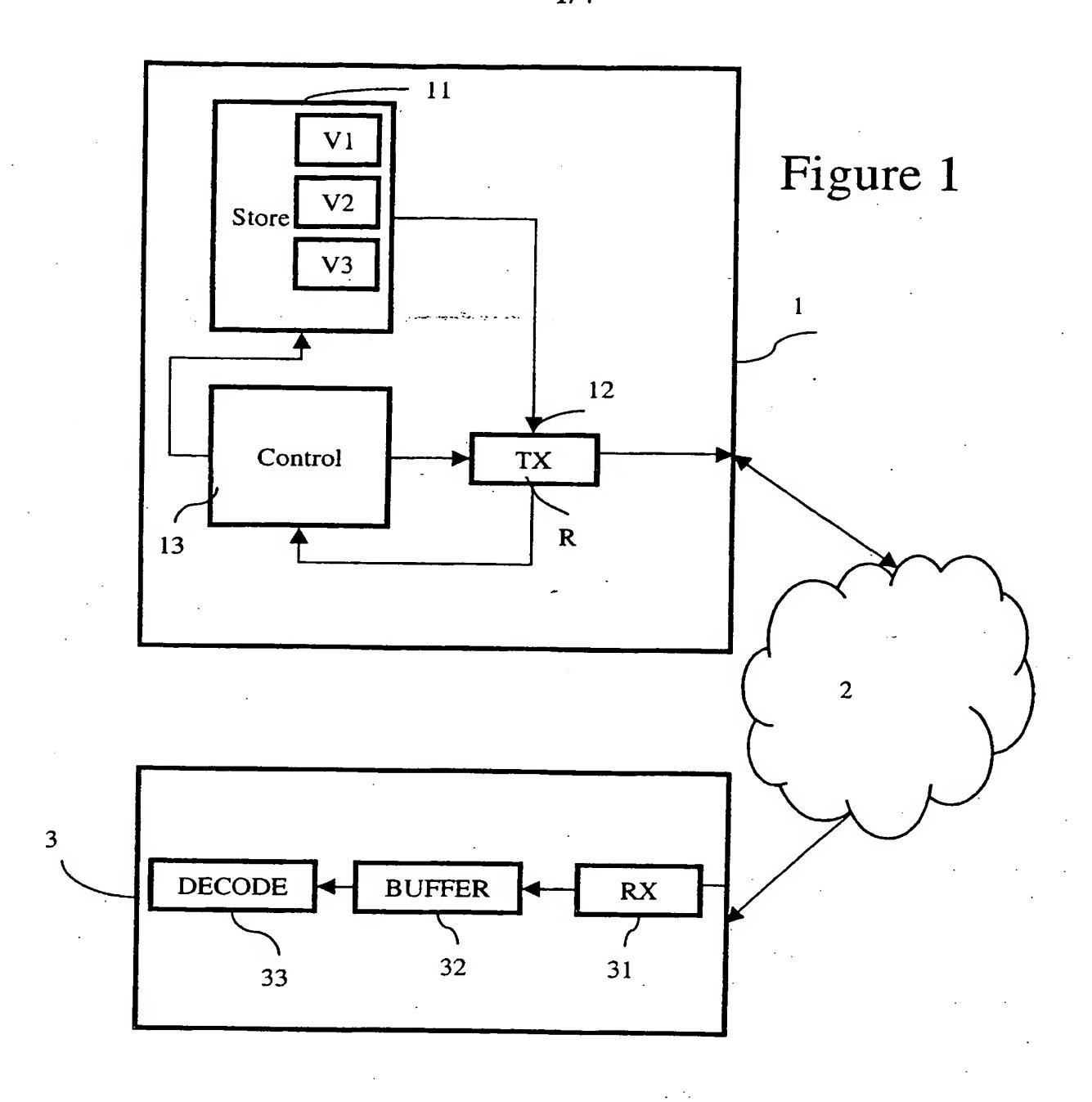
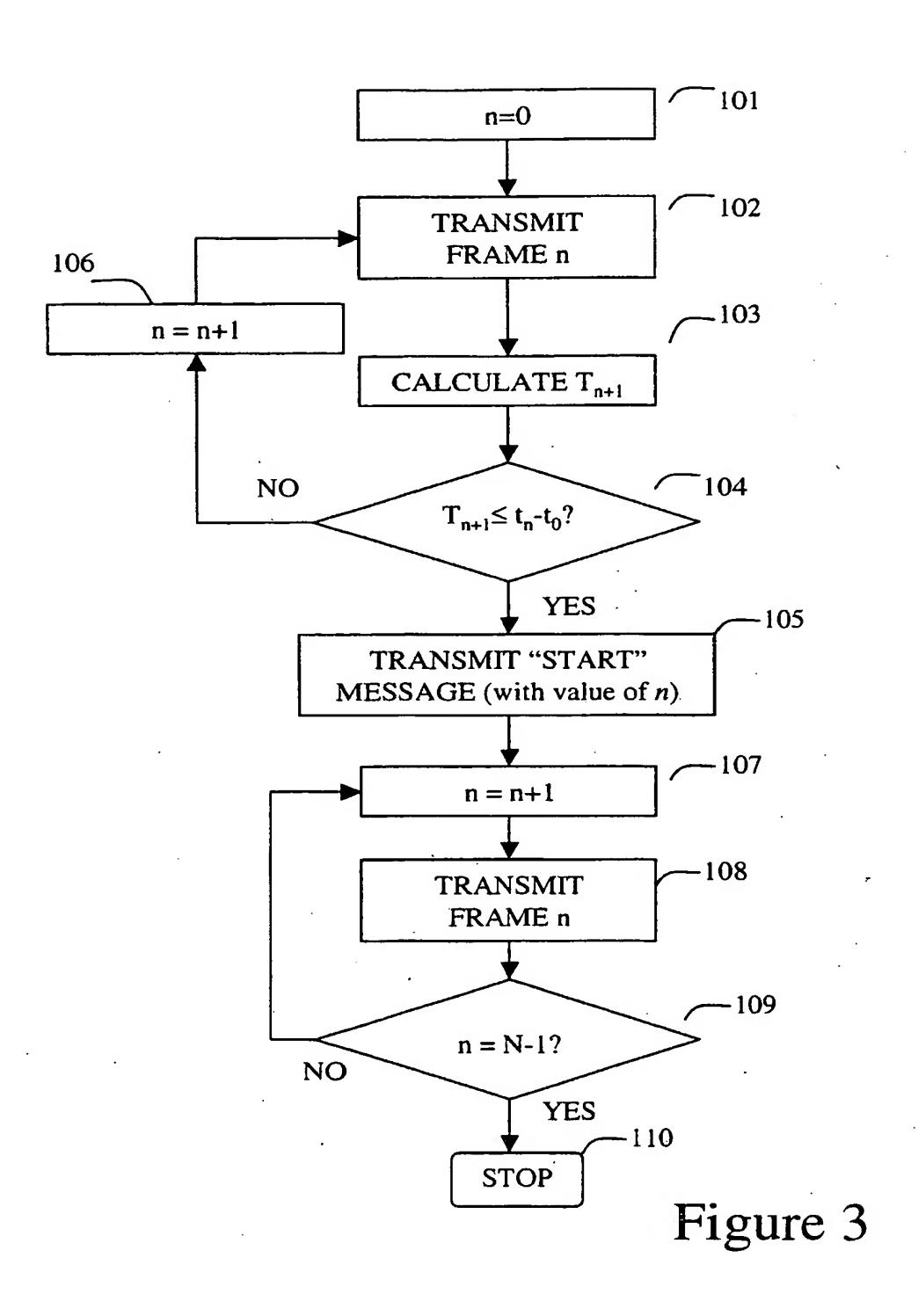
1/4



 t_0 b_0 bits ... t_i b_i bits ... t_{N-1} b_{N-1} bits

Figure 2



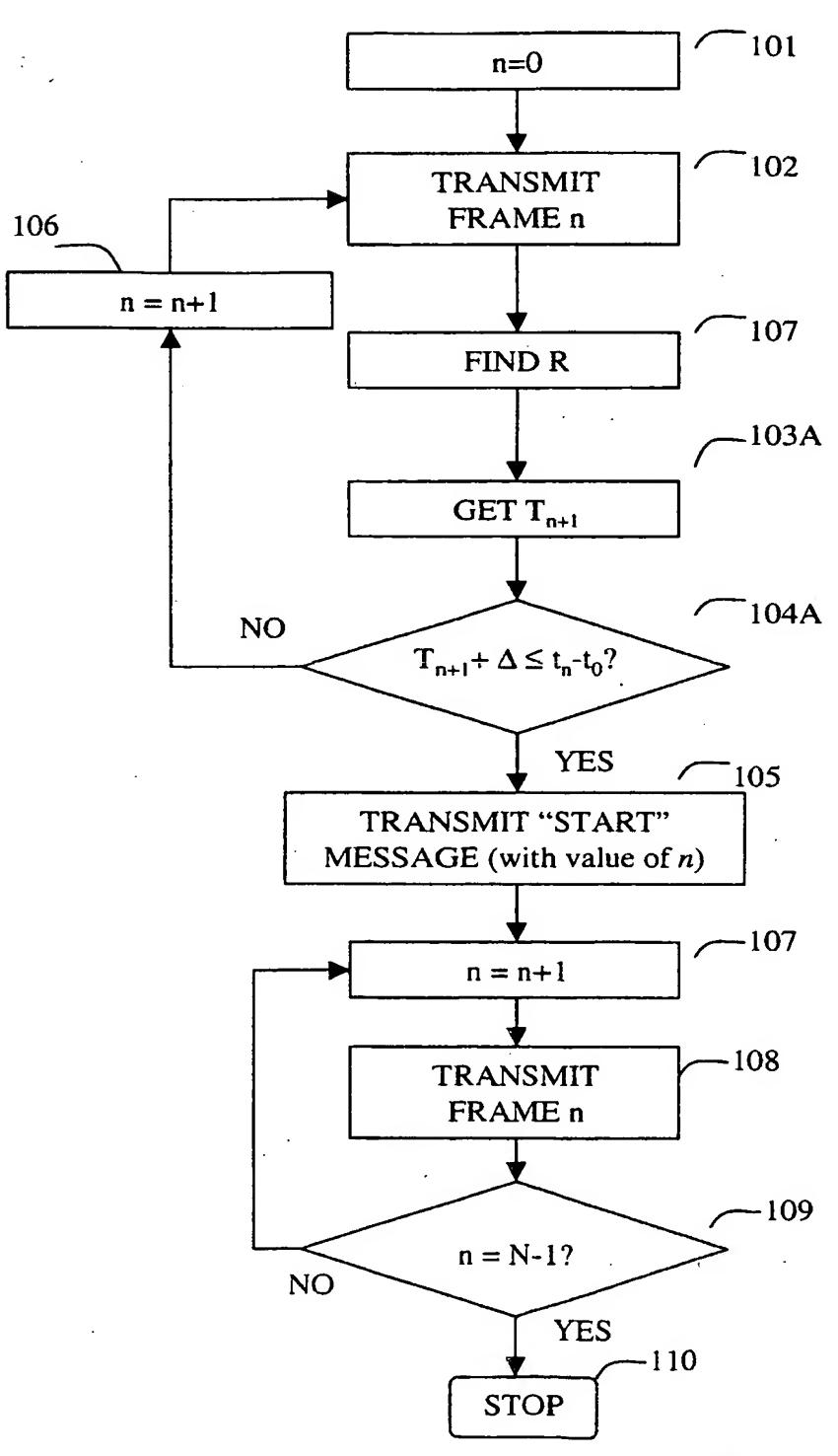


Figure 4

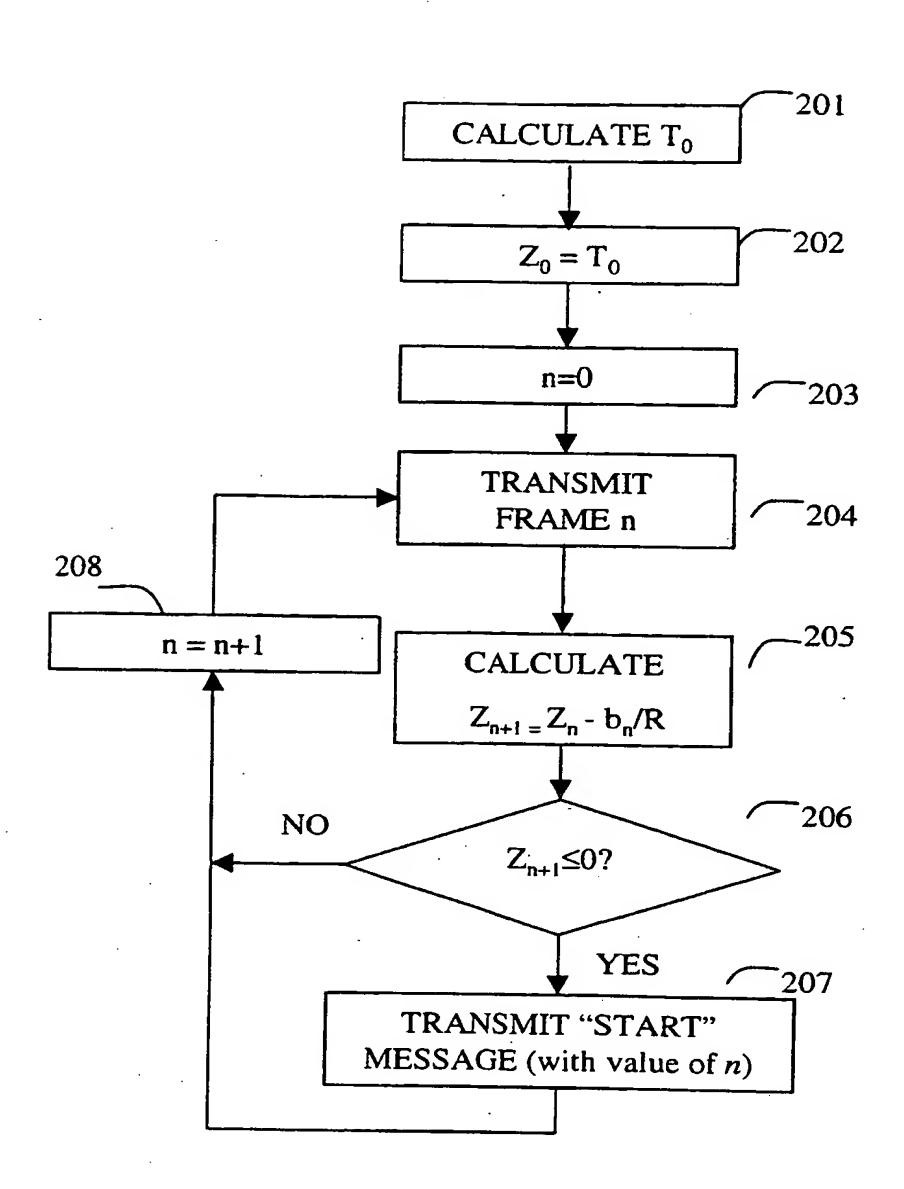


Figure 5